REMARKS

In response to the Office Action mailed September 28, 2006, Applicants respectfully request reconsideration. To further the prosecution of this Application, Applicants submit the following remarks, have amended claims and have added new claims. The claims as now presented are believed to be in allowable condition.

Claims 1-20 were pending in this Application. By this Amendment, claims 21-24 have been added. Accordingly, claims 1-24 are now pending in this Application. Claims 1, 6, 13, and 14 are independent claims.

Rejections under §102 and §103

Claims 1-20 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,774,640 (Kurio).

Applicants respectfully traverse each of these rejections and requests reconsideration. The claims are in allowable condition.

Kurio discloses a fault-tolerant computer 101 having dual fault-tolerant network controllers 311, 312. Network traffic normally flows through a primary network controller 311. (Col. 6, line 50 through Col. 7, line 6). When a severe fault occurs in the primary network controller 311, the system disables the primary network controller 311, and assigns its MAC address to a secondary network controller 312, which processes all network traffic while the primary network controller 311 is disabled. (Col. 8, lines 20-37).

Claims 1-5

Claim 1 was rejected as being anticipated by Kurio. Claim 1 is directed to a method performed by a data storage system having (i) a first storage processor, (ii) a second storage processor and (iii) a communications subsystem coupled to the first and second storage processors. The method is for operating the data storage system during a failure within the communications subsystem.

The method comprises (a) while the first and second storage processors perform data storage operations, enabling operation of the communications subsystem to provide communications between the first and second storage processors, (b) sensing a failure within a critical portion of the communications subsystem, and (c) *resetting an interfacing portion* of the communications subsystem in response to the sensed failure *to enable one of the first and second storage processors to continue operation.*

The cited reference does not teach or suggest a method having a step of *resetting an interfacing portion* of the communications subsystem in response to the sensed failure *to enable one of the first and second storage processors to continue operation.* Rather, Kurio teaches detecting a fault in a primary network interface 311, disabling that primary network interface 311, and reassigning the MAC address of the primary network interface 311 to a second network interface 312 such that all data flow between a computer and a network pass through the second network interface 312. (Col. 2, lines 42-50). This reassignment does not *enable one of the first and second storage processors to continue operation.* It is not clear if the Office Action regards the central processing units (CPUs) 301-303 or the input/output processors 304, 305 as analogous to the storage processors, but neither the CPUs 301-303 nor the input/output processors 304, 305 are *enabled to continue operation* by this reassignment process or by any other *resetting* of *an interfacing portion.* If the rejection of claim 14 is to be maintained, Applicants respectfully request that it be pointed out with particularity where the cited prior art teaches such a step of *resetting an interfacing portion* of the communications subsystem in response to the sensed failure *to enable one of the first and second storage processors to continue operation.*

For the reasons stated above, claim 1 patentably distinguishes over the cited prior art, and the rejection of claim 1 under 35 U.S.C. §102(b) should be withdrawn. Accordingly, claim 1 is in allowable condition.

Because claims 2-5 depend from and further limit claim 1, claims 2-5 are in allowable condition for at least the same reasons. Additionally, it should be

understood that the dependent claims recite additional features which further patentably distinguish over the cited prior art.

For example, claim 2 recites generating an error signal in response to *loss of a clock signal* from the *clock circuitry* within a predetermined timeout period. This feature is not taught or suggested by the cited prior art. Indeed, Kurio fails to teach any clock circuit whatsoever. If the rejection of claim 2 is to be maintained, Applicants respectfully request that it be pointed out with particularity where the cited prior art teaches such generating an error signal in response to *loss of a clock signal* from the *clock circuitry* within a predetermined timeout period.

As an additional example, claim 4 recites *opening a switch disposed between the first and second interfaces* in response to the sensed failure. This feature is not taught or suggested by the cited prior art. If the rejection of claim 4 is to be maintained, Applicants respectfully request that it be pointed out with particularity where the cited prior art teaches *opening a switch disposed between the first and second interfaces* in response to the sensed failure.

As an additional example, claim 5 recites *breaking electrical pathways between the first and second interfaces* in response to loss of one of the first and second power supply signals. This feature is not taught or suggested by the cited prior art. If the rejection of claim 5 is to be maintained, Applicants respectfully request that it be pointed out with particularity where the cited prior art teaches *breaking electrical pathways between the first and second interfaces* in response to loss of one of the first and second power supply signals.

Claims 14-20

Claim 14 was rejected as being anticipated by Kurio. Claim 14 is directed to a communications subsystem for a data storage system having a first storage processor and a second storage processor. The communications subsystem has *an interfacing portion configured to interconnect the first storage processor with the second storage processor*, *a clock circuit* coupled to the interfacing portion, and a controller coupled to the interfacing portion and the clock circuit. The

controller is configured to *enable operation of the interfacing portion to provide communications between the first and second storage processors*, sense a failure within the clock circuit, and *reset the interfacing portion* in response to the sensed failure to enable one of the first and second storage processors to continue operation.

The cited reference does not teach or suggest a communications subsystem having *an interfacing portion configured to interconnect the first storage processor with the second storage processor* and *a clock circuit* coupled to the interfacing portion. The cited reference also does not teach or suggest a controller configured to *enable operation of the interfacing portion to provide communications between the first and second storage processors* and to *reset the interfacing portion* in response to the sensed failure to enable one of the first and second storage processors to continue operation. Rather, Kurio teaches a fault-tolerant computer 101 with fault-tolerant network interfaces 311, 312. The fault-tolerant computer 101 includes three central processing units (CPUs) 301-303, two input/output processors 304, 305 (not actually depicted in the drawings, although these may be IOP 0 and IOP 1), dual memory boards 306, 307, mirrored disks 308, 309 (not actually depicted in the drawings), and two Ethernet controllers 311, 312. The fault-tolerant computer 101 also includes a control panel and dual SCSI controllers (see Fig. 3). However, nowhere does Kurio teach *an interfacing portion configured to interconnect the first storage processor with the second storage processor* or a controller configured to *enable operation of the interfacing portion to provide communications between the first and second storage processors*. Kurio does teach network interfaces 311, 312, however, these network interfaces 311, 312 do not *interconnect the first storage processor with the second storage processor* nor do they *provide communications between the first and second storage processors*. It is not clear if the Office Action regards the CPUs 301-303 or the input/output processors 304, 305 as analogous to the storage processors, but neither the CPUs 301-303 nor the input/output processors 304, 305 are interconnected by the network interfaces 311, 312.

Kurio also fails to teach a controller configured to *reset the interfacing portion*. Kurio does teach that upon detection of a severe fault in a primary network interface 311, a device driver disables the primary network interface 311, and reassigns its MAC address as well as all network traffic to a second network interface 312. (Col. 8, lines 20-37). However, as shown above, the network interfaces 311, 312 do not *interconnect the first storage processor with the second storage processor* nor do they *provide communications between the first and second storage processors*. Thus, Kurio does not teach an interfacing portion, consistent with the limitations in claim 14, that is reset. If the rejection of claim 14 is to be maintained, Applicants respectfully request that it be pointed out with particularity where the cited prior art teaches such a *resetting* of an interfacing portion that *provides communications between the first and second storage processors*.

In addition, Kurio fails to teach *a clock circuit* coupled to the interfacing portion. Indeed, Kurio fails to teach any *clock circuit* whatsoever. If the rejection of claim 14 is to be maintained, Applicants respectfully request that it be pointed out with particularity where the cited prior art teaches such a *clock circuit* coupled to the interfacing portion.

In addition, claim 14 recites limitations which are similar to those recited in claim 1. For that reason, claim 14 distinguishes over the prior art for reasons similar to those presented above in connection with claim 1.

For the reasons stated above, claim 14 patentably distinguishes over the cited prior art, and the rejection of claim 14 under 35 U.S.C. §102(b) should be withdrawn. Accordingly, claim 14 is in allowable condition.

Because claims 15-20 depend from and further limit claim 14, claims 15-20 are in allowable condition for at least the same reasons. Additionally, it should be understood that the dependent claims recite additional features which further patentably distinguish over the cited prior art.

For example, claim 16 recites an output stage *configured to provide a reset signal*. This feature is not taught or suggested by the cited prior art. If the

rejection of claim 16 is to be maintained, Applicants respectfully request that it be pointed out with particularity where the cited prior art teaches such a *reset signal*.

As an additional example, claim 17 recites a *Cache Mirroring Interface (CMI) bus*. This feature is not taught or suggested by the cited prior art. If the rejection of claim 17 is to be maintained, Applicants respectfully request that it be pointed out with particularity where the cited prior art teaches such a *CMI bus*.

As an additional example, claim 19 recites a switch coupled to the controller, the *switch being disposed between the first and second interface*. This feature is not taught or suggested by the cited prior art. Indeed, Kurio does not teach a switch anywhere. If the rejection of claim 19 is to be maintained, Applicants respectfully request that it be pointed out with particularity where the cited prior art teaches such a *switch disposed between the first and second interface*.

Claims 6-12

Claim 6 was rejected as being unpatentable over Kurio. Claim 6 is directed to a data storage system having a first storage processor, a second storage processor, and a communications subsystem. The communications subsystem has (i) an *interfacing portion interconnected between the first storage processor and the second storage processor*, (ii) *a clock circuit* coupled to the interfacing portion, and (iii) a controller coupled to the interfacing portion and the clock circuit. The controller is configured to (a) *enable operation of the interfacing portion to provide communications between the first and second storage processors*, (b) sense a failure within the clock circuit, and (c) *reset the interfacing portion* in response to the sensed failure to enable one of the first and second storage processors to continue operation.

Claim 6 recites limitations which are similar to those recited in claim 14. For that reason, claim 6 distinguishes over the prior art for reasons similar to those presented above in connection with claim 14.

For the reasons stated above, claim 6 patentably distinguishes over the cited prior art, and the rejection of claim 6 under 35 U.S.C. §102(b) should be withdrawn. Accordingly, claim 6 is in allowable condition.

Because claims 7-12 depend from and further limit claim 6, claims 7-12 are in allowable condition for at least the same reasons. Additionally, it should be understood that the dependent claims recite additional features which further patentably distinguish over the cited prior art.

Claim 13

Claim 13 was rejected as being unpatentable over Kurio. Claim 13 is directed to a data storage system having a first storage processor, a second storage processor, and a communications subsystem. The communications subsystem has (i) an *interfacing portion interconnected between the first storage processor and the second storage processor*, (ii) *a clock circuit* coupled to the interfacing portion, and (iii) a controller coupled to the interfacing portion and the clock circuit. The controller includes (a) means for enabling operation of the interfacing portion to provide communications between the first and second storage processors, (b) means for sensing a failure within the clock circuit, and (c) means for resetting the interfacing portion in response to the sensed failure to enable one of the first and second storage processors to continue operation.

Claim 13 recites limitations which are similar to those recited in claim 14. For that reason, claim 13 distinguishes over the prior art for reasons similar to those presented above in connection with claim 14.

For the reasons stated above, claim 13 patentably distinguishes over the cited prior art, and the rejection of claim 13 under 35 U.S.C. §102(b) should be withdrawn. Accordingly, claim 13 is in allowable condition.

Newly Added Claims

Claims 21-24 have been added and are believed to be in allowable condition. Claim 21 depends from claim 1. Claim 22 depends from claim 3. Claim 23 depends from claim 8. Claim 24 depends from claim 16. Support for claim 21 is provided within the Specification, for example, on page 2, lines 18-26, page 3, line 23 through page 4, line 2, and page 5, line 26 through page 6, line 2. Support for claims 22-24 is provided within the Specification, for example, on page 7, lines 4-7, page 7, lines 21-24, and Fig. 1. No new matter has been added.

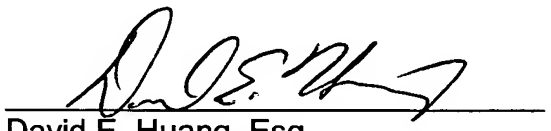
Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Amendment, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicant's Representative at the number below.

Applicants hereby petition for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this Amendment, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-3661.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 616-2900, in Westborough, Massachusetts.

Respectfully submitted,



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